PATENT APPLICATION

SMaL Camera Tech.- RPD00085

CMOS ACTIVE PIXEL WITH RESET NOISE REDUCTION

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BACKGROUND OF INVENTION

Field of the Invention

The invention relates to a CMOS image sensor array design that is capable of substantially reducing reset noise. More specifically, the invention relates to an array of active pixels having rows and columns with one amplifier for each column to produce a feedback to the reset transistors of the respective column to reduce noise.

DESCRIPTION OF THE RELATED ART

CMOS image sensors are attractive due to the compatibility with VLSI circuits. However, CMOS imagers have typically higher noise than CCD imagers. While CCD imagers employ correlated double-sampling (CDS) to remove the reset noise commonly referred to as kTC noise, the operation of most CMOS imagers does not allow true CDS. Instead, uncorrelated double-sampling is

employed to remove the constant reset level. Unfortunately, this method actually increases reset noise.

Prior art CMOS pixel designs disclose correlated-doubling sampling incorporated in the pixel design. Although this circuit substantially removes the reset noise, an amplifier and two additional devices are necessary within each pixel to provide the CDS function, greatly increasing the area of the pixel. What is needed is a CMOS image sensor array design where each active pixel in the image sensor array does not need a separate amplifier .

SUMMARY OF THE INVENTION

A CMOS image sensor array has rows and columns of active pixels. In addition, there are one or more column lines each cooperating with the active pixels in the respective columns. Each active pixel in a column has an output connected to the column line. Each active pixel includes a photodiode that produces a signal proportional to incident light intensity. The proportional signal may be current, voltage, or charge. The proportional signal is applied to the active pixel output if the column select and row select are appropriately set. In addition, each active pixel has a reset transistor to reset the pixel. Each reset transistor has a gate and first and second terminals. A reset voltage is applied to the gate of each reset transistor to reset the transistors.

The CMOS image sensor array also has one or more amplifiers . Each amplifier has a first input connected to the column line. Each amplifier also provides a negative feedback output to the first terminal of each reset transistor of the active pixels for the respective cooperating column line. A reset reference voltage is applied to a second input of each amplifier to adjust the negative feedback to set the voltage at the second terminal of each reset transistor to a desired reset voltage. The second terminal of each reset transistor cooperates with the first input of the respective amplifier for the column.

The voltage at each said second terminal is V_T -ΔV below the reset voltage, where ΔV keeps the reset transistor in the subthreshold region in the steady state of the reset phase. The ΔV typically exceeds one hundred millivolts.

The CMOS image sensor array has one or more row lines each cooperating with the active pixels in a row. Each active pixel in the row has a row select transistor coupled between its respective second terminal and the first input of the respective amplifier.

The CMOS image sensor array further has a source follower transistor coupled between the second terminal and the row select transistor of each active pixel.

The first advantage of the present invention is that it provides a CMOS imager design that is capable of substantially reducing the reset noise.

A second advantage of the present invention is that it provides a reset noise reduction without substantially increasing the complexity of the pixel. More specifically, the present invention avoids the inclusion of an amplifier in each pixel.

DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic drawing of a prior art standard active pixel.

FIG. 2 shows a schematic drawing of an active pixel and amplifier according to the present invention.

FIG. 3 shows a schematic drawing of the equivalent circuit of FIG 2 for noise analysis.

FIG. 4a shows a schematic drawing of the arrangement of pixels, amplifiers, and various signals in an 2x2 array of pixels with a column feedback arrangement.

FIG. 4b shows a schematic drawing of the arrangement of pixels, amplifiers, and various signals in an 2x2 array of pixels with a row feedback arrangement.

Fig. 5 shows a schematic drawing of one embodiment of the amplifier of the invention shown in FIG.2.

Fig. 6 shows a schematic drawing of a circuit for generating a reset voltage for the active pixel of FIG. 2.

Fig. 7 shows a schematic drawing of second embodiment of the amplifier of the invention shown in FIG.2.

Fig. 8 shows a schematic drawing of a third embodiment of the amplifier of the invention shown in FIG 2.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows a schematic diagram of a standard active pixel. A first circuit, for example, a photocircuit such as a photodiode 11 produces a current proportional to the incident light intensity. The photocircuit could alternatively produce a proportional voltage or charge. The resulting photocurrent is integrated on a charge sensing capacitor 13. The charge-sensing capacitor 13 may be any source of capacitance, but is typically a parasitic reverse-biased PN junction capacitance associated with the photodiode 11 itself. A MOS transistor 15 operates as a source follower that buffers the voltage on the capacitor 13 nondestructively to a column line 23. A row select MOS switch 17 activates the source follower transistor 15 when the particular row is selected. When the pixel is reset, the gate 21 of the reset transistor 19 is brought up to, typically, Vdd. The charge sensing capacitor 13 is reset to approximately Vdd-Vt where Vt is the threshold voltage of reset transistor 19. The reset level contains error from pixel to pixel. The error has two components. The first component is fixed error due to

mismatches in Vt and transistor sizes. The other component is the random reset noise on the order of $\sqrt{\frac{kT}{C}}$ where C is the charge sensing capacitor 13. There are two different modes of reset; hard reset and soft reset. In hard reset, the gate of the rest transistor is pulled up more than Vt higher than the drain voltage. In this mode, the reset transistor behaves as a resistor producing thermal noise. In soft reset, the gate of the reset transistor is held at a lower potential so that the reset transistor behaves as a diode, producing shot noise. It has been shown that hard reset modes produce random noise on the order of $\sqrt{\frac{kT}{C}}$ while soft reset contributes $\sqrt{\frac{kT}{2C}}$. Since they differ only by a small amount, only hard reset is considered for simplicity in the following anaylsis. During reset, the reset transistor 19 behaves as a resistor with resistance value R that depends on the size of the transistor, the threshold voltage V_T, and the gate drive. The thermal noise spectral density of a resistor with a value R is given by

$$S_R(f) = 4kTR \qquad (1)$$

Since the resistor R and the capacitor C constitute a low-pass filter, the noise spectral density at Node 1 (i.e.first node) (27) is

$$S_1(f) = 4kTR \cdot \frac{1}{1+(2\pi fRC)^2} \qquad (2)$$

The mean square noise at Node 1 (27) is found by integrating $S_1(f)$ over frequency;

$$\overline{v}_1^2 = \int_0^\infty S_1(f)df = 4kTR\int_0^\infty \frac{1}{1+(2\pi fRC)^2}df \qquad (3)$$

Since $\int_0^\infty \frac{1}{1+(2\pi fRC)^2} df = \frac{1}{4RC}$, (4)

Giving the mean-square noise

$$\overline{v}_1^2 = \frac{kT}{C} \quad (5)$$

The rms value of the reset noise is thus $\sqrt{\frac{kT}{C}}$. For a typical sense capacitor value of 10 fF, the rms noise $\overline{v}_1 = 643\,\mu V$ at room temperature.

In principle, both the fixed and random error components can be removed by correlated double sampling (CDS). In CDS, the pixel voltage is first measured immediately following the reset. This measures the reset level error including both components. The first measurement (the reset value) is stored in either analog of digital form. After the integration period, the pixel voltage is remeasured. Since the pixel is not reset again before the second measurement, the second measurement contains the same error components introduced upon reset plus change in voltage in response to light. The first measurement is subtracted from the second measurement (the integrated value) leaving only the light response term, thus removing the errors. One drawback of CDS is that the first measurement must be stored for the duration of the integration period. Since the integration period can approach the frame period, the storage circuit must be able to hold the value for this period. For a typical 30 frames/s imager, the maximum storage period is 33ms. Analog sample-and-hold circuits would require large hold capacitors to achieve such a long hold time. Moreover, since each pixel's reset value must be stored, CDS requires the reset values for the entire array of pixels be stored. A frame buffer is thus necessary. An analog frame buffer requires a large amount of chip area and power consumption. For this reason, most frame buffers are digital. Digital frame buffers also consume large chip area and are expensive.

To circumvent the problems associated with the CDS, most CMOS imagers employ UDS (uncorrelated double sampling). In this method, the reset measurement corresponding to the next frame is subtracted instead of the reset measurement of the current frame. Since the reset for the next frame occurs immediately after the second measurement of the current frame, there is no need for long storage of measurements. Typically, the measurements are held in capacitors in switched-capacitor subtractor. Although UDS removes the fixed error due to Vt and transistor size mismatches, is does not reduce the random $\frac{kT}{C}$ reset noise. This is because the reset noise introduced during the reset for the next frame is not correlated with the reset noise of the current frame. Since two uncorrelated noise quantities are present after the subtraction, UDS actually increases total reset noise power by a factor of two.

Fig. 2 shows a pixel 31 and an amplifier 33 according to the present invention. Amplifier 33 may, for example, be a differential amplifier. The dashed line represents the pixel 31.

Referring to Fig.2, the structure of pixel 31 is identical to the standard pixel in Fig. 1, except the first terminal 35 (i.e. drain) of the reset transistor M1 (37) is connected to the output of the amplifier A (33) instead of V_{DD}. The second terminal of reset transistor M1 (37) is the source and is the same as NODE 1 (27). The first and second terminals 35 and 27 being designated as a drain or source may be interchanged depending on the transistor type and design. During the reset phase, the select signal RS 40 (i.e. in this case a row select signal) on the gate 41 of row select transistor M3 (43) is brought high typically to V_{DD}, and a reset voltage V_{RESET}, typically V_{DD}, is applied to RESET (i.e. gate 45 on reset transistor 37). The loop consisting of the amplifier A (33), M1(37), and the source follower M2 (47) and the row select transistor M3 (43) is a unity-gain loop. The voltage V_R (i.e. reset reference voltage) applied to the non-inverting input 49 of the amplifier A (33) is determined such that Node 1 (27) is servoed to a voltage V_T-ΔV below

the reset voltage by the negative feedback loop (i.e. output of amplifier 33 to drain 35 of reset transistor 37). ΔV is on the order of a few hundred millivolts in order to keep M1 (37) in the subthreshold region in the steady-state of the reset phase. It can be shown that the required $V_R = V_{RESET}-(V_T-\Delta V) +V_{GS2}+V_{DS3}$ (where V_{GS2} is the gate to source voltage for source follower M2 (47) and V_{DS3} is the drain to source voltage for row select transistor M3 (43). Since M1 (37) is in subthreshold region, its drain-to-source resistance r_{ds1} is very large. Therefore, the dominant pole in the feedback loop is determined by r_{ds1} and the pixel capacitance C (50). The amplifier A (33) preferably has much wider bandwidth than the dominant pole frequency so as not to compromise the stability of the loop. Once the pixel reaches a steady-state, RESET (45) is pulled down, sampling and holding the voltage at Node 1 (27). Ideally, this voltage would be equal to $V_{RESET}-(V_T-\Delta V)$. However, when M1 (37) is turned off, charge is injected from M1 (37) to C (50) resulting in an offset voltage. This constant offset voltage is of little concern as long as its value is the same pixel-to-pixel. There is a small variation of charge injection due to mismatches in transistor and capacitor sizes. Such variation is typically random and below the typical noise floor, and thus is not noticeable, or can be cancelled by a number of techniques. Thermal noise sampled on Node 1 (27) is greatly reduced by the feedback loop. Fig. 3 illustrates the equivalent circuit for the noise analysis. The transistors produce thermal noise with spectral density as before,

$$S_R(f) = 4kTR \qquad (6)$$

For simplicity of analysis, we assume that M2, M3, and I (51) behave as an ideal source follower with unity gain and no noise. Since both the amplifier and the source follower have large capacitive loads, noise in these circuits can be ignored in practice. Using node analysis, the voltage at Node 1 (27) is calculated to be

$$v_1 = \frac{v_n}{1+A} \qquad (7)$$

were A is the gain of amplifier A (33)

Thus, noise spectral density of v_1 is;

$$S_1(f) = \frac{S_R(f)}{(1+A)^2} = \frac{4kTR}{(1+A)^2} \qquad (8)$$

The mean square value of noise voltage at Node 1 (27) can be computed by integrating the noise spectral density over the bandwidth determined by R (52) and C (55);

$$\overline{v_1^2} = \int_0^\infty \frac{4kTR}{(1+A)^2} \cdot \frac{1}{1+(2\pi fRC)^2} df = \cdot \frac{1}{(1+A)^2} \frac{kT}{C} \qquad (9)$$

When the reset switch M3 (43) is turned off, the mean-square reset noise sampled is identical to (9). Compared with the standard reset noise in (5), the mean-square noise is reduced by a factor of $(1+A)^2$, the rms noise by $(1+A)$. For moderate gain A of 9 for example, the reset noise is reduced by a factor of 10. Compared with UDS, the noise reduction corresponds to a factor of $10\sqrt{2} \approx 14$. The additional factor of $\sqrt{2}$ is due to doubling of noise power in standard UDS.

A 2x2 pixel example is shown in Fig.4a in order to illustrate the arrangements of pixels, amplifiers, and various signals in an array of pixels. Pixels 31a and 31b receive the output from amplifier 33a at one terminal of reset transistors 37a and 37b. Similarly, pixels 31c and 31d receive the output from amplifier 33b at one terminal of reset transistors 37c and 37d. The output of pixels 31a and 31b (i.e. from row select transistors 43a, 43b respectively) are provided to one input of differential amplifier 33a. The output of pixels 31c and 31d (i.e. from row select transistors 43c, 43d respectively) are provided to an input of differential amplifier 33b. Reset 45a is provided to the gates of reset transistors 37a and 37c. Reset 45b is provided to the gates of reset transistors 37b and 37d. Row select signal 40a is provided to row select transistors 43a and 43c. Row select signal 40b is provided to row select transistors 43b and 43d.

It would be within the skill of the art to interchange the rows and columns and their respective circuit array designs shown in FIG. 4a. FIG 4b shows an array with the rows and columns interchanged. Pixels 31b and 31d receive the output from amplifier 33a at one terminal of reset transistors 37b and 37d. Similarly, pixels 31a and 31c similarly receive the output from amplifier 33b at one terminal of reset transistors 37a and 37c. The output of pixels 31b and 31d (i.e. from column select transistors 43b, 43d respectively) are provided to one input of differential amplifier 33a. The output of pixels 31a and 31c (i.e. from column select transistors 43a, 43c respectively) are provided to a second input of differential amplifier 33b. Reset 45b is provided to the gate of reset transistors 37a and 37d. Reset 45a is provided to the gate of reset transistors 37c and 37d. Column select signal 40b is provided to row select transistors 43a and 43b. Row select signal 40a is provided to row select transistors 43c and 43d.

Fig. 5 shows one embodiment of the amplifier A (33) with a differential input. The amplifier includes the circuitry shown outside pixel 31. The left half of the differential input of amplifier A (33) is made up of transistors M2 (47) and M3 (43) inside pixel (31). The source of M3 (43) is connected to Node 1 through M3 (43) when the row select RS of transistor M3 (43) is high for this row. The right half of the differential input consists of V_R (49), which is applied to the gate of transistor M2A (60) (i.e. second differential amplifier input transistor) in series with transistor M3A (62). M3 (43) and M3A (62) function as source degeneration resistors for the differential input pair consisting of M2 (47) and M2A (60). The current through M2A is mirrored by the current mirror comprising M4A (64) and M5A (66). The output of the amplifier, Node 2 (70), is connected to the drain of reset transistor M1 (37) in the manner described above in conjunction with Fig. 2. In order for the feedback loop to be stable, the frequency of the dominant pole that is determined by the on-resistance of M1 (37) and the sense capacitor C (55) must be lower at least by a factor of gain A compared with non-dominant poles. The

non-dominant poles are given by the Thevenin resistance and the parasitic capacitance at Node 2 (70), and those at Node 3 (72).

The reset voltage V_R (49) is V_T-ΔV below V_{DD}, and can be generated by a circuit shown in Fig. 6. ΔV is a positive voltage so that the reset transistor remains in subthreshold region. The size of transistor MR (76) and the current I_3 is set in such way that it is biased in subthreshold region and $V_R=V_{DD}-(V_T-\Delta V)$.

A second embodiment of the amplifier A (33) is shown in Fig. 7. This embodiment includes an additional amplifier a_o (80) and an NMOS transistor M7A (82). The amplifier a_o (80) keeps the drain voltages of M2A (60) and M4A (64) at the reset voltage V_R (49), so that the drain-to-source voltages of M4A (64) and M2A (60) are matched to that of M5A (66) and M7A (82), respectively. This improves the input referred offset voltage of the amplifier A (33). The transistor M6A (64) prevents Node 2 (70) from falling far below the reset voltage V_R (49) during the transient. If the voltage on Node 2 (70) drops too far below V_R (49), the drain-source resistance of the reset transistor M1 (37) is reduced. This causes the dominant pole frequency to go up potentially causing instability.

Fig. 8 shows a third embodiment of the invention. In this embodiment, the amplifier is configured differently during the read phase so that it works as a unity-gain follower. During the reset phase, switches S1 (90) and S4 (92) are closed, S2 (94) and S3 (96) are open, S5 (98) in the right position, and S6 (100) in the up position. The circuit thus configured is identical to that in Fig. 7, and the reset is performed in the same manner. During the read phase, the switch positions are reversed, S1 (90) and S4 (92) are open, S2 (94) and S3 (96) are closed, S5 (98) in the left position, and S6 (100) in the down position. This configures the circuit into a unity-gain follower so that the output voltage at Node 4 (102) is a reproduction of the voltage on the sense node (Node 1 (38)). It can be shown that the offset voltage of the unity-gain follower configured in this manner is substantially the same as that during the reset mode. Since this offset voltage is

already stored in the sense capacitor, the effect is automatically cancelled in a manner similar to standard offset cancellation.

While the preferred embodiments of the invention have been shown and described, numerous variations and alternative embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.